

REMARKS

In the Office Action, the Examiner rejected Claims 1-5, 7-10 and 13-15, which are all of the pending claims, under 35 U.S.C. 112, first paragraph, on the grounds that the specification is not sufficiently enabling. None of the claims was rejected over the prior art.

The rejection of the claims is respectfully traversed. Claims 1, 2, 3, 5, 7, 10 and 15 are being amended to improve the form and readability of the claims.

After carefully studying the claims and the specification, it is believed that the specification fully enables those of ordinary skill in the art to practice the claimed invention. Accordingly, the rejection of the claims is respectfully traversed.

Applicants' invention, generally, relates to synchronizing the frequency of a local clock of a digital data decoder with the frequency of a program clock. As discussed in detail in the present application, in situations where compressed data are transmitted to a decoder, the frequency of the program clock and the frequency of the local clock on the decoder need to be kept reasonably close together in order to properly decompress the data.

The present invention addresses this issue, and does so in a manner that places reduced demand on the processor used to keep the clock frequencies together. More specifically, in accordance with Applicants' invention, under some circumstances, the frequency of the two clocks are brought together using hardware, and in other circumstances, software, running on the processor, is used to bring these two frequencies closer together. Figure 7 of the application illustrates one embodiment of the hardware

that may be used, and Figure 9 of the application illustrates a software procedure that may be used

With this procedure of Applicants' invention, the processor is only called upon under specific conditions to address the frequency differences between the program and local clocks.

Applicants' invention uses information contained in the Program Clock Reference (PCR) fields transmitted to the decoder, and also information generated about the local clock, referred to as the System Time Clock (STC) value. The PCR fields are well known in the field and are discussed in the Background section of the application.

In rejecting the claims, the Examiner raised questions about several limitations in Claims 1, 2 3, 7 and 13. Specifically, the Examiner questioned whether there is enablement or support in the specification for:

- i) determining the differences between the local and program clock frequencies before adjusting those frequencies;
- ii) the decoder receives the program clock signals; and
- iii) determining the absolute difference between the local clock value and the program clock value.

With particular regard to Claim 1, the Examiner commented that with the procedure shown in Fig. 7, the frequency is adjusted only when there is a difference between the values stored in the PCR register 701 and the STC register 704.

Applicants invention involves determining the frequency difference between the program and system clocks, and one specific implementation of that invention is to use the values from the PCR and STS registers to determine that frequency difference. As explained in the present application, the difference between the PCR and STC values is not the same as the frequency difference between the program and system clocks, but that frequency difference can be calculated using the PCR and STC values.

Moreover, the determination of this frequency difference is done before adjusting the frequency of the local clock.

In the Office Action, the Examiner noted that the left hand side of Figure 9 includes the step of "Calculate difference in clock rate (frequency)," while the right hand side of Figure 9 includes the step of "Calculate difference in PCR and STC values."

These steps are discussed in the specification from page 26, line 27 to page 27, line 16. There, it is explained that the difference between these two steps is that the step on the left uses previously stored STC and PCR values, while the step on the right uses recently received STC and PCR values. In both steps, however, the difference between the local and program clock frequencies are determined by using the STC and PCR values; and, moreover, both of these steps are done prior to adjusting the frequency at which the local clock oscillates.

The procedure for adjusting the clock frequency is also discussed in the specification from page 25, line 29 to page 26, line 10. In this portion of the specification, it is explained that the clock difference is used to generate an output that, in turn, is used to regulate a voltage controlled oscillator. This oscillator is used to adjust the frequency of the local clock.

With regard to Claim 2, the Examiner asked which portion of the specification teaches that the decoder receives the program clock signals, and which portions of the specification teach that the hardware performs each recited step.

The first of these issues is explained in the discussion of the MPEG 2 system on pages 4-6 of the application. In this portion of the specification, it is explained that the program clock recovery (PCR) data, which is shown in Figure 2, is in the MPEG 2 bitstream, and that this bitstream is applied to decoder 301, shown in Figure 3. Control data, including the PCR data, are then applied to the system time clock generator, which includes the system time clock (STC). Accordingly, this step is clearly explained and supported in the application.

The hardware for performing these functions is shown in Fig. 7 and is described in, among other places, in the specification from page 25, line 19 to page 26, line 19.

With respect to the reference to the “absolute difference” between the local and program clock values, it is noted that this term is used in the specification on page 14, line 26. This “absolute difference” refers to the difference between the PCR time stamp and the system time clock, which is discussed on page 28, lines 4 and 5. The word “absolute” is used to distinguish this difference from the frequency difference between the local and program clock frequencies, which is also described in the claims.

It may be helpful to note that the disclosed embodiment of Applicants’ invention involves two differences between the program clock and the system clock. One difference is the difference between the frequencies of the two clocks. The second difference is the difference between the times of these two clocks, and is referred to as the absolute difference between the clocks.

Regarding Claim 3, the Examiner asked that the Applicant indicate which portions of the specification: teach the step of determining the difference between the local and program clock frequencies before the step of adjusting, teach that the decoder receives the program clock signals, and teach determining the absolute difference between the local clock value and the program clock value.

Each of these issues has been specifically addressed above, and it is not necessary to repeat that discussion.

In rejecting Claim 7 the Examiner objected to the limitation that the decoder receives the clock signals at a program clock frequency. Claim 7 is herein being amended to indicate that these received clock signals specify the program clock frequency.

The Examiner also asked, in connection with Claim 7, which portions of the specification teach: i) means for determining the difference between the local and program clock frequencies before the means for adjusting, and ii) means for determining the absolute difference between the local and program clock values. Each of these issues was specifically addressed above, and it is not necessary to repeat that discussion.

With respect to Claim 13, the Examiner here too asked which portion of the specification teaches means for determining the difference between the local and program clock frequencies before the means for adjusting. This issue has been discussed above, and it is not necessary to repeat that discussion here.

For the reasons advanced above, the specification provides clear, enabling support for the claimed invention. The Examiner is thus asked to reconsider and to withdraw the rejection of Claims 1-5, 7-10 and 13-15 under 35 U.S.C. 112, and to allow these claims.

Every effort has been made to place this application in condition for allowance, a notice of which is requested. If the Examiner believes that a telephone conference with Applicants' Attorneys would be advantageous to the disposition of this case, the Examiner is asked to telephone the undersigned.

Respectfully submitted,

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